UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,939	01/16/2004	Craig Hansen	43876-153	4645

7590 02/01/2011

McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
MOLL, JESSE R	
ART UNIT	PAPER NUMBER
2181	
MAIL DATE	DELIVERY MODE
02/01/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,939	HANSEN ET AL.	
	Examiner	Art Unit	
	JESSE R. MOLL	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/17/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-28 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-10 of U.S. Patent No. 7,430,655 in view of claims 1-68 of Patent No. 7,516,308 and over claims 1-68 of Patent No. 7,516,308 in view of claims 1-10 of U.S. Patent No. 7,430,655.

For example,

Claim 1 Recites:	Patent 7,516,308 Discloses:	Patent 7,430,655 Discloses:
A programmable processor comprising: a data path capable of transmitting data; an external interface operable to receive data from an external source and communicate the received data over the data path;	A processor comprising: a virtual memory addressing unit; a data path (claim 1) an external interface operable to receive data from an external source and communicate the received data over the data path; a cache operable to retain data communicated between the external interface and the data path. (claim 25)	
a register file containing a plurality of registers each having a register width,	register file comprising a plurality of registers coupled to the data path (claim 1)	
the register file coupled to the data path and configured to support processing of a plurality of threads		A method of executing a plurality of threads within a single programmable processor (claim 1)

Claim 1 Recites:	Patent 7,516,308 Discloses:	Patent 7,430,655 Discloses:
and to store a plurality of multiple-bit data elements in partitioned fields, each of the multiple-bit data elements having an elemental width smaller than the register width;		the method comprising: storing a plurality of data elements in partitioned fields of at least one register having a register width, each of the data elements having an elemental width smaller than the register width (claim 1)
an execution unit coupled to the data path, the execution unit configured to execute a plurality of instruction streams from the plurality of threads in a multistage pipeline such that the multistage pipeline is capable of including instructions from different ones of the instruction streams in different stages of the multistage pipeline,		receiving an instruction stream for each one of the plurality of threads at an execution unit; and executing instructions from each instruction stream received at the execution unit in a multistage pipeline such that, at a given time, the multistage pipeline includes instructions from different ones of the instruction streams in different stages of the multistage pipeline (claim 1)
each instruction stream including a single arithmetic instruction that specifies an arithmetic operation to cause multiple instances of the arithmetic operation to be performed,		the instructions including a single instruction that specifies an operation to cause multiple instances of the operation to be performed (claim 1)
each instance of the arithmetic operation to be performed using a different one of the plurality of multiple-bit data elements in partitioned fields of at least one of the registers to produce a catenated result,		each instance of the operation to be performed using a different one of the plurality of data elements in partitioned fields of the at least one register to produce a catenated result (claim 1)

Claim 1 Recites:	Patent 7,516,308 Discloses:	Patent 7,430,655 Discloses:
the single arithmetic instruction causing a plurality of multiple-bit data elements in partitioned fields to be read in parallel from a register included in the register file,	the execution unit capable of executing group floating-point operations in which multiple floating-point operands stored in partitioned fields of one or more of the plurality of registers (claim 1)	
and causing the catenated result to be written in parallel to one of the registers included in the register file;	wherein the catenated results are returned to a register in the plurality of registers. (claim 7)	
and wherein each of the multiple-bit data elements has an elemental width, and the data path has a data path width multiple times greater than the elemental width,	wherein an elemental width of the floating-point operands is equal to or less than a width of the data path (claim 1)	
to allow multiple-bit data elements used for the multiple instances of the arithmetic operation to be transmitted in parallel from the register file to the execution unit, and wherein the execution unit is operable to receive, in parallel, multiple-bit data elements for the multiple instances of the arithmetic operation	the group floating-point operations involve operating on at least two of the multiple floating-point operands in parallel. (claim 2) *also, see below*	
and execute the multiple instances of the arithmetic instruction to produce the catenated result.	executing group floating-point operations… are operated on to produce catenated results (claim 1)	

3. It was commonly known in the art and would have been obvious for one of ordinary skill in the art to have transmitted the multiple elements in parallel. The use of

parallel data transfer is extremely common in processors. For example, when reading from RAM, multiple bytes are read in parallel to increase performance. In this case, it would have been obvious for one of ordinary skill in the art to have allowed multiple elements in parallel from the register file to the execution unit because the elements are operated on in parallel and would clearly benefit from parallel transfer.

The claimed invention is generally directed to a processor containing elements present in the claims of the '308 and '655 patents. Combining the elements of executing multi-operation instructions ('655 Patent) and transferring the concatenated results ('308 Patent) would have been obvious for one of ordinary skill in the art at the time of the invention, yielding predictable results, because a processor which executes many operations simultaneously would benefit from storing the results simultaneously as well (also, see above).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JESSE R. MOLL whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 10:00 am - 6:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571)272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jesse R Moll
Examiner
Art Unit 2181

/J. R. M./
Examiner, Art Unit 2181

/Chun-Kuan Lee/
Primary Examiner, Art Unit 2181